Investigation of III-V Semiconductor Heterostructures for Next-generation CMOS

Abstract

This work is aimed towards the growth and characterization of III-V semiconductor heterostructure and their application in next-generation Complementary Metal Oxide Semiconductor (CMOS) devices. The two main components of this study will include the integration of III-V compounds on silicon for tunnel-junction Esaki diodes, and the investigation of carrier transport properties for III-V channel CMOS development in the 6.1 Å lattice constant family. The integration of III-V compound semiconductors with Si can combine the cost advantage and maturity of the Si technology with the superior performance of III-V materials. We intend on investigating high quality epitaxial growth of GaAs and GaSb on Si (001) wafers through the use of various buffer layers including AlSb and crystalline $SrTiO_3$. Multiple characterization tools including in-situ Reflection High Energy Electron Diffraction (RHEED), high resolution XRD, AFM, and TEM will be employed to study the properties of the grown structures with the fabrication and electrical characterization of broken gap Esaki diodes. The III-V material system centered at the 6.1 Å lattice parameter (a_0) is a promising candidate for future high frequency, low voltage CMOS. Channel materials based on In and As/Sb will be explored by employing Hall measurements to investigate the impact of uniaxial stress on carrier density and mobility of InAs-based quantum well structures of CMOS materials for the first time. In-situ optical characterization of these MBE grown InAs-based heterostructures will be performed using reflectance anisotropy spectroscopy (RAS).

BIO-

Originally from New Delhi, India, Kunal received his Bachelors in Physics from Angelo State University in 2010 and then went on to get his Masters in Electrical & Computer Engineering from the University of Missouri in Columbia where he developed a novel platform based on plasmonic nanostructures for fluorescence based bio-sensing and bio-imaging using conventional soft lithography and RF sputtering techniques.

He is currently pursuing his PhD in Materials Science, Engineering & Commercialization at Texas State University and working on numerous projects which include the integration of III-V compounds on Silicon for high frequency, low

power Tunnel Field-Effect Transistors (TFETs) and Esaki diodes using solid-source MBE, studying the quantitative effect of uniaxial strain on carrier transport properties in III-V semiconductor channels for next-generation CMOS, as well as in-situ optical characterization of quaternary heterostructures using reflectance anisotropy spectroscopy (RAS).

High Performance Long Wave Infrared (LWIR) Focal Plane Array (FPA) Sensor for Missile Defense

Technical Abstract

Antimony (Sb) based strained layer superlattice (SLS) and unipolar barrier long wave infrared detector designs show promise of increased performance over state of the art detectors when implemented in large focal plane array formats (> 512 x 512 elements). We propose to develop strain-compensated T2SL FPAs with interface engineering and novel AR coatings to improve the overall device quantum efficiency. By introducing an interface layer of 1 ML thick InSb in the

T2SL structure, the overall tensile strain can be compensated to improve the crystal quality and the performance of the epitaxial device structure. A nanostructured, graded-index antireflective (AR) coating is added to the T2SL FPAs device to enable significant reduction of light reflection to improve the external quantum efficiency.